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Priority Date: 8/24/00 Other:

Name Mohammad Ali
AU 2177 Examiner # 78414
Room # 4718 Phone 605-4356
Serial # 09/934,657

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What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

file operation with the namespace & the operation involve in execution of an application.

Keywords:
"file operation" same "back-up operation" without
"corresponding task execution" same
"file path" same "namespace cache"

STIC Searcher Teresa Esterhold Phone 308-7795
Date picked up 6/9/04 11:30am Date Completed 6/9/04 2:15pm

Search and Information Resources Administration

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Set      Items   Description
S1     4614455   OPERATION? OR FUNCTION? OR INSTRUCTION? OR EXECUTION? OR C-
             OMMAND?
S2       89064   S1 (2N)(FILE? ? OR DATABASE OR DATA()BASE OR INFORMATION OR
              DATA OR LOOKUP OR LOOK()UP)
S3        8842   (WITHOUT OR "NOT")()(SUSPEND? OR DELAY? OR HOLD? OR DEFER?
             OR STAY? OR TABLE? OR WAIT? OR SHELV?)
S4     2765615   S1 (2N)(TASK? OR JOB OR JOBS OR FUNCTION? OR ROLE? OR ASSI-
             GNMENT? OR CHORE? OR DUTY OR DUTIES)
S5      829732   URL OR URLS OR (UNIVERSAL OR UNIFORM)()RESOURCE()LOCATOR? -
             OR NAMESPACE OR DOMAIN OR ADDRESS? OR FILE()PATH?
S6      117822   S1 (2N) (EXECUTION? OR ATOMIC? OR TRANSACTION? OR ACTIVIT?)
S7           0   S2 AND S3 AND S4 AND S5 AND S6
S8          14   S2 AND S3 AND S4
S9           0   S8 AND S7
S10          1   S8 AND S5
S11         38   S2 AND S3
S12         14   S11 AND S4
S13          4   S11 AND S5
S14         17   S8 OR S10 OR S12 OR S13
S15         14   S14 NOT PY>2000
S16         14   S15 NOT PD>20000824
S17         14   RD (unique items)
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         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/May W3
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/May W4
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
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Descriptors: database management systems
Identifiers: database management systems DBS-25; IDMS
Class Codes: C7100 (Business and administration)

17/5/11 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04052934 JICST ACCESSION NUMBER: 99A0497096 FILE SEGMENT: JICST-E
A study on data base restructuring methods in SDF.
ITO HIDEFUMI (1); NAKAMURA TOSHIRO (1); ITAKURA ICHIRO (1)
(1) Ntt Johoryutsupurattofomuken
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1999, VOL.99,NO.34(SSE99 1-6), PAGE.13-18, FIG.9, TBL.2, REF.4
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.394/.395
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The SDF, which is one of the **functional** elements in Intelligent Network, manages various types of service **data** necessary for **execution** of IN services. Since the service data are generally extensive and also contain data which can be updated, it is desirable to manage them by using a data base. This paper, at the premise to apply a data base to the management of service data in SDF, puts demanded conditions to the system which executes IN services in order, and describes the data base management methods and their inplementation which can meet the conditions. Furthermore, by bringing the data base restructuring methods in focus, which enables flexible alteration of data structure **without suspending** any services, this paper shows their basic mechanism, composition methods of application program for data restructuring, recovering methods in data destruction detection, etc. (author abst.)
DESCRIPTORS: information service; intelligent network; network management; DBMS; reconstitution; crash recovery; backup
BROADER DESCRIPTORS: service; communication network; information network; network; communication administration; management; computer application system; system; constitution; restoration; action and behavior
CLASSIFICATION CODE(S): ND11010T

17/5/12 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00982202 I96045433230
Irregular sampling for spline wavelet subspaces
(Irregulaere Erfassung fuer Spline-Wavelet-Unterraeume)
Youming Liu
Dept. of Appl. Math., Beijing Polytech. Univ., China
IEEE Transactions on Information Theory, v42, n2, pp623-627, 1996
Document type: journal article Language: English
Record type: Abstract
ISSN: 0018-9448

ABSTRACT:
Spline wavelets psi (ind m)(t) are important in time-frequency localization due to (i) psi (ind m) can be arbitrarily close to the optimal case as m is sufficiently large, (ii) psi (ind m) has compact support and simple analytic expression, which lead to effective computation. Although the spline wavelet subspaces are so simple, Walter's well-known sampling theorem does **not hold** if the order of spline m is even. Moreover, when irregular sampling is considered in these spaces, it is hard to determine the sampling density, which is a serious problem in applications, in this

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Set     Items   Description
S1    3089559   OPERATION? OR FUNCTION? OR INSTRUCTION? OR EXECUTION? OR C-
            OMMAND?
S2     116906   S1 (2N)(FILE? ? OR DATABASE OR DATA()BASE OR INFORMATION OR
             DATA OR LOOKUP OR LOOK()UP)
S3      11283   (WITHOUT OR "NOT")()(SUSPEND? OR DELAY? OR HOLD? OR DEFER?
            OR STAY? OR TABLE? OR WAIT? OR SHELV?)
S4     896675   S1 (2N)(TASK? OR JOB OR JOBS OR FUNCTION? OR ROLE? OR ASSI-
            GNMENT? OR CHORE? OR DUTY OR DUTIES)
S5     307266   URL OR URLS OR (UNIVERSAL OR UNIFORM)()RESOURCE()LOCATOR? -
            OR NAMESPACE OR DOMAIN OR ADDRESS? OR FILE()PATH?
S6     113327   S1 (2N) (EXECUTION? OR ATOMIC? OR TRANSACTION? OR ACTIVIT?)
S7          1   S2 AND S3 AND S4 AND S5 AND S6
S8         49   S2 AND S3 AND S4
S9          5   S8 AND S5
S10        12   S8 AND S6
S11       297   S2 AND S3
S12        57   S11 AND S5
S13        18   S12 AND S6
S14        33   S7 OR S9 OR S10 OR S13
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
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14/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06089653 **Image available**
SIMULATION **EXECUTION** METHOD, **EXECUTION** DEVICE AND RECORDING MEDIUM

PUB. NO.: 11-031169 [JP 11031169 A]
PUBLISHED: February 02, 1999 (19990202)
INVENTOR(s): SUZUKI TAKESHI
APPLICANT(s): OKI ELECTRIC IND CO LTD
APPL. NO.: 09-199391 [JP 97199391]
FILED: July 09, 1997 (19970709)
INTL CLASS: G06F-017/50; G01R-031/28; G06F-011/26

ABSTRACT

PROBLEM TO BE SOLVED: To process information so that it is **not delayed** from a job scheduled termination period by obtaining respective allowance time based on the job scheduled termination periods and **job** predicted **execution** time on plural pieces of information to be processed and processing information in order from that having the least allowance time.

SOLUTION: Information processed for respective jobs are stored in a storage part 11 by giving the job scheduled termination periods. A calculation circuit 14 calculates **job** predicted **execution** time on **information** preserved in the storage part 11 and it calculates allowance time based out calculated **job** predicted **execution** time and **job** scheduled termination period on information. Plural pieces of information preserved in the storage part 11 are rearranged in order from the least allowance time in accordance with calculated allowance time by a sorting part 15. An operation processing part 12 reads information form the head of the storage part 11, namely from the least allowance time, sequentially processes them with a simulation program and outputs the result and a condition to a data base part 13.

14/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04495171 **Image available**
PARALLEL COMPUTERS

PUB. NO.: 06-139071 [JP 6139071 A]
PUBLISHED: May 20, 1994 (19940520)
INVENTOR(s): NAKANISHI CHIKAKO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-292693 [JP 92292693]
FILED: October 30, 1992 (19921030)
INTL CLASS: [5] G06F-009/38; G06F-009/38; G06F-013/16
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1788, Vol. 18, No. 441, Pg. 99, August 17, 1994 (19940817)

ABSTRACT

PURPOSE: To realize the data by-pass circuit of a memory access instruction in parallel computers.

CONSTITUTION: A super scalar processor 20 is constituted of an instruction fetching stage 4, an instruction decoding stage 5, plural **functional** units 6 to 9 having pipeline structure respectively, a register file 3 to hold temporarily data to be used for executing an **instruction**, a memory **data** by-pass 10, and a data by-pass 12, and it can access the data memory

2 of the outside through a data bus 11. One **functional** unit is constituted of an **execution** stage 61, a memory access stage 62 and a write back stage 63. Thus, the data can be transferred between pipelines **without waiting** for the data to be written in a memory, and further, the data can be transferred to the pipeline requesting the read memory data, and the finish of a read instruction need not be waited.

14/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04189946 **Image available**
ARITHMETIC UNIT

PUB. NO.: 05-181646 [JP 5181646 A]
PUBLISHED: July 23, 1993 (19930723)
INVENTOR(s): TSUNATORI YUICHI
APPLICANT(s): NEC OFF SYST LTD [486651] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-000449 [JP 92449]
FILED: January 07, 1992 (19920107)
INTL CLASS: [5] G06F-007/548; B41J-002/485; G06F-007/00; G06F-015/31; G06F-015/66; G09G-005/36
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 29.4 (PRECISION INSTRUMENTS -- Business Machines); 44.9 (COMMUNICATION -- Other); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1638, Vol. 17, No. 602, Pg. 72, November 05, 1993 (19931105)

ABSTRACT

PURPOSE: To shorten the time in case of executing repeatedly an operation by outputting an arithmetic result from a storage part as for **data** whose **operation** is executed once by adding a storage part to a computing element.

CONSTITUTION: When a coordinate 13 and a trigonometrical **function** 17 are inputted, an **address** is generated by a decoder 11, and given to a storage part 12. The storage part 12 outputs data by this **address** , refers to an existence flag by a control circuit 15 with respect to its data, outputs an arithmetic result 16, when the arithmetic result is set already, outputs a result from a multiplying circuit 14 as the arithmetic result 16, when the operation is not executed yet, and simultaneously, stores it in the storage part 12. Also, in a second time and thereafter, when the coordinate 13 and the trigonometrical **function** 17 of the same combination are inputted, the control circuit 15 outputs the arithmetic result 16 **without waiting** for the result of the multiplying circuit 14.

14/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03466625 **Image available**
INSTRUCTION PROCESSING SYSTEM FOR INFORMATION PROCESSOR

PUB. NO.: 03-129525 [JP 3129525 A]
PUBLISHED: June 03, 1991 (19910603)
INVENTOR(s): YAMAGATA MAKOTO
SHIMIZU NAOHIKO
SHIBATA MASABUMI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-268631 [JP 89268631]
FILED: October 16, 1989 (19891016)
INTL CLASS: [5] G06F-009/38

JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1245, Vol. 15, No. 344, Pg. 103, August 30, 1991 (19910830)

ABSTRACT

PURPOSE: To rapidly execute a branch instruction by preparing the 3rd instruction for specifying which is the 2nd instruction to be executed next to the 1st instruction and executing the 3rd instruction prior to the **execution** of the 1st instruction.

CONSTITUTION: Two registers TAR0, TAR1 are prepared as target **address** registers(TARs) 5 observed from a program in order to hold branched **addresses** . A load target **address** (LTA) instruction and a branch target on condition(BTC) instruction are respectively prepared as an instruction for loading a branched **address** to the TARs 5 and an **instruction** for branching **data** to an **address** specified by the TARs 5. Since an individual instruction can execute pipeline processing **without delaying** it through the number of instructions is increased, the processing performance of the information processor is improved.

14/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02627334 **Image available**
JOB EXECUTION CONTROL SYSTEM

PUB. NO.: 63-244234 [JP 63244234 A]
PUBLISHED: October 11, 1988 (19881011)
INVENTOR(s): TAKAHATA NOBUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-077832 [JP 8777832]
FILED: March 31, 1987 (19870331)
INTL CLASS: [4] G06F-009/46
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 824, Vol. 13, No. 54, Pg. 20, February 08, 1989 (19890208)

ABSTRACT

PURPOSE: To execute a job by self-system when other systems are currently operating or the load is large by updating **execution** system **information** that is included in job description information.

CONSTITUTION: Another system state display part 2 that displays the operating state of other systems in a console 8 by referring to the operating information of respective systems and an **execution** system **information** updating part 3 that changes **execution** system **information** 6 included in job description informa tion 5 to make it able to be executed by the self-system, are provided. When another system is not operating or in overload state, such suitable job descrip tion information 5 as executable by the self-system is selected out of another system **execution job** description **information** 5 entered in a start waiting job table 4, and the **execution** system **information** 6 in the information 5 is changed, then executed by the self-system. As a result, a job designated for the **execution** by another system can be executed by the self-system **without waiting** for a long time for the **execution** .

14/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02611335 **Image available**
JOB EXECUTION CONTROL SYSTEM

PUB. NO.: 63-228235 [JP 63228235 A]
PUBLISHED: September 22, 1988 (19880922)
INVENTOR(s): TAKAHATA NOBUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-061862 [JP 8761862]
FILED: March 17, 1987 (19870317)
INTL CLASS: [4] G06F-011/16; G06F-015/16; G06F-015/16
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 816, Vol. 13, No. 30, Pg. 83, January 24, 1989 (19890124)

ABSTRACT

PURPOSE: To execute a job designated to be executed in other system in its own system **without waiting** it for a long time by automatically updating an **execution** system **information** included in a job descriptive information.

CONSTITUTION: In case an abnormality occurs in a designated **execution** system, if an information to instruct the **execution** of the **job** is designated in the other system, an abnormality, if occurring in the other system, is detected by an other-system's state supervising part 2. And a corresponding **execution** system **information** is automatically updated by an **execution** system **information** updating part 3, so that the **job** whose **execution** is designated to the other system is executed by the self system without intermediation by an operator. In such a way, when a job for which an instruction to permit a proxy **execution** by other systems is preliminarily issued, the job is automatically executed by the other system when an abnormality occurs in a certain system.

14/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

02074132 **Image available**
OUTPUT INSTRUCTION CONTROL SYSTEM

PUB. NO.: 61-288232 [JP 61288232 A]
PUBLISHED: December 18, 1986 (19861218)
INVENTOR(s): BABA YASUO
HANAZAWA AKIO
SATO MASAO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-131005 [JP 85131005]
FILED: June 17, 1985 (19850617)
INTL CLASS: [4] G06F-011/00; G06F-013/10
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 577, Vol. 11, No. 153, Pg. 61, May 19, 1987 (19870519)

ABSTRACT

PURPOSE: To start the **execution** of the next instruction **without waiting** for the response from a peripheral device by providing registers where the **address** of an output instruction executed for the peripheral device by an arithmetic unit and **data** indicating the **execution** result of the output instruction are held.

CONSTITUTION: When the output instruction to the peripheral device is executed, the instruction **address** is stored in a lagging **address** register 7, and the **address** and data information to the peripheral device are set to an I/O instruction **address** register 9 and an I/O **instruction data** register 10 and are sent to the peripheral device. Though the end signal of the output instruction is returned normally from

nearly always already in or still in the queue and so are inherited **without delay** . The instruction queue unit has an instruction queue buffer (IQB), pre-fetch unit (PFU), fetch unit (FU) and pre-decode unit (PDU).

ADVANTAGE - Reduces pauses to minimum for non **address** sequential program **execution** , several **command** sequences are stored at same time independent of each other in instruction queue. Instruction queue also useable as command cache.

Dwg.1/1

Title Terms: PROCESS; FETCH; COMMAND; PROGRAM; CONTROL; UNIT; MICROPROCESSOR; MICRO; CONTROL; SELECT; BRANCH; SPECIFIC; LOCATE; INSTRUCTION; QUEUE; WRITING; INSTRUCTION; DATA; QUEUE; READ; INSTRUCTION; DATA; QUEUE

Derwent Class: T01

International Patent Class (Main): G06F-009/30; G06F-009/32; G06F-009/38

International Patent Class (Additional): G06F-009/06; G06F-012/02

File Segment: EPI

14/5/18 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012437350 **Image available**

WPI Acc No: 1999-243458/199920

XRPX Acc No: N99-181195

Instruction fetch unit in single instruction **multiple** data **(SIMD) processor**

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)

Inventor: PARK H C; HEON C B; NGUYEN L T; PARK H

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5889986	A	19990330	US 97790028	A	19970128	199920	B
KR 98069857	A	19981026	KR 9735007	A	19970725	199952	
KR 267101	B1	20001002	KR 9735007	A	19970725	200134	

Priority Applications (No Type Date): US 97790028 A 19970128

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5889986	A		8	G06F-009/06	
KR 98069857	A			G06F-009/38	
KR 267101	B1			G06F-009/38	

Abstract (Basic): US 5889986 A

NOVELTY - The instruction in main buffer (212) of program buffer (210) is selected and transferred to a decoder by a selection circuit via an instruction register (230). A control circuit transfers the instruction sequence from branch target buffer (216) to main buffer after last instruction is transferred from main buffer to decoder.

DETAILED DESCRIPTION - The program buffer (210) including main and secondary buffers (212,214) is coupled to a selection circuit. The branch target buffer (216) is coupled to main buffer. A prefetch circuit which has an instruction bus (205) with a data width equal to storage capacity of main buffer is coupled to scan logic (250) and secondary buffer. The prefetch circuit fetches an instruction sequence including an instruction at a target **address** for a flow control instruction found by scan logic and stores the instruction sequence in the secondary buffer. The branch target buffer coupled to main buffer has the storage capacity same as that of main buffer. An INDEPENDENT CLAIM is included for processor operating method.

USE - In single **instruction** multiple **data** (SIMD) processor that uses a RISC-type instruction set.

ADVANTAGE - Instruction sequence from secondary buffer is transferred to main buffer to maintain stream of instructions **without delay** for instruction memory access by prefetching instructions into secondary buffer while instructions are being transferred from main buffer. All the three buffers can be filled with instructions in a

single clock cycle as they all have identical storage capacity and bus between the buffers and **instruction** memory has **data** width equal to storage capacity of each buffer. Searching more instruction allows earlier detection of flow control instructions and provides more time for fetching the branch target **instruction** before **execution** of branch **instruction** is required.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of instruction fetch unit.

Instruction bus (205)
Program buffer (210)
Main buffer (212)
Secondary buffer (214)
Branch target buffer (216)
Instruction register (230)
Scan logic (250)
pp; 8 DwgNo 2/3

Title Terms: INSTRUCTION; FETCH; UNIT; SINGLE; INSTRUCTION; MULTIPLE; DATA; SIMD; PROCESSOR
Derwent Class: T01
International Patent Class (Main): G06F-009/06; G06F-009/38
File Segment: EPI

14/5/19 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011526169 **Image available**
WPI Acc No: 1997-502655/199746
Related WPI Acc No: 1990-036987; 1997-414930
XRPX Acc No: N97-419041

Direct match data flow memory for parallel processor - includes storage locations containing memory words with first parameter storing indicator of parameter received as input with flag representing state of first memory word and associated operation

Patent Assignee: DAVIDSON G S (DAVI-I); GRAFE V G (GRAF-I)
Inventor: DAVIDSON G S; GRAFE V G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5675757	A	19971007	US 88223133	A	19880722	199746	B
			US 90559523	A	19900724		
			US 95403612	A	19950314		

Priority Applications (No Type Date): US 88223133 A 19880722; US 90559523 A 19900724; US 95403612 A 19950314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5675757	A		28	G06F-013/00	Cont of application US 88223133 Div ex application US 90559523 Div ex patent US 5465368

Abstract (Basic): US 5675757 A

The data flow memory includes numerous storage locations, each associated with a unique physical **address** . Each storage location includes at least three memory words of variable width. A first parameter memory word stores a first parameter indicator of a first data parameter received as input data. This parameter is selected from a group containing a logical value and an arithmetic value.

An opcode memory word stores an operation to be performed on the first parameter. A first flag memory word associated with the first parameter memory word has a state representative of the presence of the parameter in the first memory word and the operation to be performed when the first parameter is present. A first recycle indictor memory word indicates that the first parameter is always available.

ADVANTAGE - Allows **execution** of **instruction** as soon as it arrives at processor **without waiting** for further **data** or

instruction fetches.
Dwg.5/11
Title Terms: DIRECT; MATCH; DATA; FLOW; MEMORY; PARALLEL; PROCESSOR; STORAGE; LOCATE; CONTAIN; MEMORY; WORD; FIRST; PARAMETER; STORAGE; INDICATE; PARAMETER; RECEIVE; INPUT; FLAG; REPRESENT; STATE; FIRST; MEMORY; WORD; ASSOCIATE; OPERATE
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

14/5/20 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011437023 **Image available**
WPI Acc No: 1997-414930/199738
Related WPI Acc No: 1990-036987; 1997-502655
XRPX Acc No: N97-345842

Direct match data flow machine for processor node architecture - includes processor with control logic and direct match data flow memory having storage locations for parameter indicator, operation indicator, flag indicator and recycle indicator

Patent Assignee: SANDIA CORP (SAND-N)
Inventor: DAVIDSON G S; GRAFE V G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5657465	A	19970812	US 88223133	A	19880722	199738	B
			US 90559523	A	19900724		
			US 95403603	A	19950314		

Priority Applications (No Type Date): US 88223133 A 19880722; US 90559523 A 19900724; US 95403603 A 19950314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5657465	A		26	G06F-013/00	Cont of application US 88223133 Cont of application US 90559523 Cont of patent US 5465368

Abstract (Basic): US 5657465 A

The data flow machine includes a processor also comprising control logic and data paths operatively connecting at least one **execution** unit, an input unit, a flag checking and updating unit and a transmission unit. A direct match data flow memory is in a one-to-one operative connection to the processor, the direct match data flow memory having a number of storage locations, each storage location having an **address** and a number of storage areas.

The storage areas further include a parameter storage area for storing at least one parameter indicator, an operation storage area storing an operation indicator of an operation to be performed on at least one of the parameter indicators,

a flag storage area having a state representative of the presence of parameter indicators required by the operation. At least one recycle indicator storage area stores a recycle indicator having a state set to indicate that a parameter indicator is always present.

ADVANTAGE - Can execute instructions as soon as they arrive at processor **without waiting** for further **data** or **instruction** fetches.

Dwg.1/11
Title Terms: DIRECT; MATCH; DATA; FLOW; MACHINE; PROCESSOR; NODE; ARCHITECTURE; PROCESSOR; CONTROL; LOGIC; DIRECT; MATCH; DATA; FLOW; MEMORY; STORAGE; LOCATE; PARAMETER; INDICATE; OPERATE; INDICATE; FLAG; INDICATE; RECYCLE; INDICATE
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

14/5/21 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011269708 **Image available**
WPI Acc No: 1997-247611/199723
XRPX Acc No: N97-204120

Virtual device support for CPU and devices - involves initiating and completing execution of command immediately with respect to virtual device without waiting for data to come during subsequent bus transfers

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: GENTRY D E
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 772130	A1	19970507	EP 96117001	A	19961023	199723	B
JP 9325947	A	19971216	JP 96307547	A	19961105	199809	
US 5848293	A	19981208	US 95552802	A	19951103	199905	
EP 772130	B1	20020814	EP 96117001	A	19961023	200255	
DE 69622960	E	20020919	DE 622960	A	19961023	200269	
			EP 96117001	A	19961023		

Priority Applications (No Type Date): US 95552802 A 19951103
Cited Patents: 2.Jnl.Ref; EP 205949; EP 539313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 772130	A1	E	18	G06F-013/10	
Designated States (Regional): DE FR GB NL SE					
JP 9325947	A		14	G06F-015/163	
US 5848293	A			G06F-013/00	
EP 772130	B1	E		G06F-013/10	
Designated States (Regional): DE FR GB NL SE					
DE 69622960	E			G06F-013/10	Based on patent EP 772130

Abstract (Basic): EP 772130 A

The method involves **atomically** transferring **command** and **data information** to a device by transferring **command data** across the data bus to the device. **Address** data is transferred across the **address** bus to the device.

This data has a device **address** , an **address** of a virtual device register, the type of command to be performed and an identification of the virtual device the command is to be performed on. The device latches the transferred data across the data and **address** buses and transfers the virtual device identification, the type of **command** and **command data** to the virtual device register. The device logic performs the command using the **command data** stored in the register.

USE - Relates to field of cache memory and to high speed caches and command processing.

ADVANTAGE - Enables transfers of **commands** and **data atomically** . Ensures device state is consistent during **command execution**

Dwg.5/9

Title Terms: VIRTUAL; DEVICE; SUPPORT; CPU; DEVICE; INITIATE; COMPLETE; EXECUTE; COMMAND; IMMEDIATE; RESPECT; VIRTUAL; DEVICE; WAIT; DATA; SUBSEQUENT; BUS; TRANSFER
Derwent Class: T01
International Patent Class (Main): G06F-013/00; G06F-013/10; G06F-015/163
International Patent Class (Additional): G06F-013/12; H04L-012/28
File Segment: EPI

14/5/22 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010971729 **Image available**
WPI Acc No: 1996-468678/199647
XRPX Acc No: N96-394933
Command execution **for** data **processing system - by publishing command in memory required in transmitting memory block to cache in state of exclusion when block is not held by cache exclusively**
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: LE H Q; SO K; TRUONG B
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8234981	A	19960913	JP 95311881	A	19951130	199647	B
US 5699538	A	19971216	US 94352467	A	19941209	199805	

Priority Applications (No Type Date): US 94352467 A 19941209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8234981	A		10	G06F-009/38	
US 5699538	A		10	G06F-009/312	

Abstract (Basic): JP 8234981 A
The method involves publishing a storage data required when storing data in a memory. A memory **address** is formed. A touch command demanding the exclusion possession of a memory block corresp. to the memory **address** is formed in a cache. The formation of the touch command is stopped when the cache holds the block exclusively.
The command required in transmitting the block to the cache in the state of exclusion is published in the memory when the cache does **not hold** the block exclusively. The data is written in the cache when all data published before the store command has been completely executed.
ADVANTAGE - Provides definite consistency model to obtain performance of weak consistency model in multi-processing system.
Dwg.2/3
Title Terms: COMMAND; EXECUTE; DATA; PROCESS; SYSTEM; PUBLICATION; COMMAND; MEMORY; REQUIRE; TRANSMIT; MEMORY; BLOCK; CACHE; STATE; EXCLUDE; BLOCK; HELD; CACHE; EXCLUDE
Derwent Class: T01
International Patent Class (Main): G06F-009/312; G06F-009/38
International Patent Class (Additional): G06F-012/08; G06F-015/16
File Segment: EPI

14/5/23 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010691103 **Image available**
WPI Acc No: 1996-188059/199619
XRPX Acc No: N96-157354
Information processing system for high speed instruction processing - has loading controller to receive loaded and writes in data register during execution of instruction for loading data from external memory
Patent Assignee: NEC CORP (NIDE)
Inventor: UCHIDA K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5504869	A	19960402	US 94275389	A	19940715	199619	B

Priority Applications (No Type Date): JP 93197754 A 19930716
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5504869	A		24	G06F-009/30	

Abstract (Basic): US 5504869 A
The system includes a token storing device (14) for storing control tokens. An arithmetic processing device (11) executes instructions in

Microprocessor super-scaler for parallel processing - uses by-pass line to interconnect pipelines and transfers data from one pipeline for subsequent processing by another

Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: ANDO H; IKENAGA C
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4207148	A1	19921224	DE 4207148	A	19920306	199301	B
US 5636353	A	19970603	US 92828277	A	19920130	199728	
			US 94225265	A	19940407		
US 6233670	B1	20010515	US 92828277	A	19920130	200129	
			US 94225265	A	19940407		
			US 97865308	A	19970529		

Priority Applications (No Type Date): JP 91144560 A 19910617
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4207148	A1		13	G06F-009/38	
US 5636353	A		12	G06F-009/38	Cont of application US 92828277
US 6233670	B1			G06F-009/38	Cont of application US 92828277
					Cont of application US 94225265
					Cont of patent US 5636353

Abstract (Basic): DE 4207148 A

The super-scaler processor (10) includes a command fetching stage (2); a command decoder stage (3) and **functional** units (4-7), all of which have a pipeline structure. Each **functional** unit includes an **execution** stage (41), a memory access stage (42) and a write-back stage (43). The **functional** units are interconnected via a by-pass line (12).

Data contained in one **functional** (pipeline) are fed via the by-pass line to another **functional** unit (pipeline) for the **execution** of subsequent **commands** . The processed **data** are transferred between pipelines without passing through a register file, so that the pipeline dealing with the processed data need **not wait** for **execution** by the other pipeline.

ADVANTAGE - Time required to execute command is reduced.

Dwg.1/8

Title Terms: MICROPROCESSOR; SUPER; SCALE; PARALLEL; PROCESS; BY-PASS; LINE ; INTERCONNECT; PIPE; TRANSFER; DATA; ONE; PIPE; SUBSEQUENT; PROCESS
Derwent Class: T01
International Patent Class (Main): G06F-009/38
File Segment: EPI

14/5/29 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008822834 **Image available**
WPI Acc No: 1991-326847/199145
XRPX Acc No: N91-250371

Computer system with cache memory - has buffering arrangement contg. mechanism for formation of pipeline of addresses

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: BROWN E W; PETOLINO J
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4114053	A	19911031	DE 4114053	A	19910429	199145	B
GB 2244158	A	19911120	GB 913954	A	19910226	199147	
US 5283890	A	19940201	US 90516322	A	19900430	199406	
			US 9312621	A	19930202		
GB 2244158	B	19940907	GB 913954	A	19910226	199433	
JP 3407808	B2	20030519	JP 91121865	A	19910425	200334	

Priority Applications (No Type Date): US 90516322 A 19900430; US 9312621 A 19930202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5283890	A		8	G06F-013/14	Cont of application US 90516322
GB 2244158	B		2	G06F-012/08	
JP 3407808	B2		7	G06F-012/08	Previous Publ. patent JP 7121437

Abstract (Basic): DE 4114053 A

A computer system with a cache memory buffers the data for storage in the cache memory and tests the cache memory to determine whether it contains the information which is to be accessed. A device for location of cache faults terminates a storage **operation** before the **information** leaves the buffer.

The buffering arrangement (20-24) contains a mechanism for formation of a pipeline of **addresses** to be accessed and the data to be stored under these **addresses** .

USE/ADVANTAGE - Enables increased operating speed to be achieved and esp. reduction in delay associated with storage instructions. (7pp Dwg.No.1/2

Title Terms: COMPUTER; SYSTEM; CACHE; MEMORY; BUFFER; ARRANGE; CONTAIN; MECHANISM; FORMATION; PIPE; **ADDRESS**
Derwent Class: T01
International Patent Class (Main): G06F-012/08; G06F-013/14
International Patent Class (Additional): G06F-009/34; G06F-012/12
File Segment: EPI

14/5/30 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008420367 **Image available**
WPI Acc No: 1990-307368/199041
XRPX Acc No: N90-236317

Computer execution **history recorder for treating processor incidents - uses pointer value recorder and** address **region mask with controller for deciding appropriate recording action and recording method**

Patent Assignee: NEC CORP (NIDE)
Inventor: NAKANO H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2643474	A	19900824	FR 901893	A	19900216	199041	B
US 5146586	A	19920908	US 90479379	A	19900213	199239	

Priority Applications (No Type Date): JP 8936370 A 19890217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5146586	A		5	G06F-011/00	

Abstract (Basic): FR 2643474 A

The device records the **execution** events in an information processor, and includes a microprogram for recording commands (1), and a device (2) for temporarily storing the commands from the microprogram. A device (10) records the value of an **address** pointer, and registers (11, 12) record the start and finish **addresses** of a mask, and the mask state. A device (7) also records the **execution data** , and the state of various logical signals.

A controller controls the **operation** of the **execution data** recorder (7) in response to the state of the mask. If set, the value of the pointer is incremented and recorded in the pointer recorder (10). Various processes for recording the **execution** history of the processor are selected by the controller depending on the value of the pointer and the value and position of the mask.

USE/ADVANTAGE - For recording incidents occuring in processor. Less memory reliant.

Dwg.1/1
Title Terms: COMPUTER; EXECUTE; HISTORY; RECORD; TREAT; PROCESSOR; INCIDENT ; POINT; VALUE; RECORD; **ADDRESS** ; REGION; MASK; CONTROL; DECIDE; APPROPRIATE; RECORD; ACTION; RECORD; METHOD
Derwent Class: T01
International Patent Class (Main): G06F-011/00
International Patent Class (Additional): G06F-009/22
File Segment: EPI

14/5/31 (Item 23 from file: 350)

008149986 **Image available**
WPI Acc No: 1990-036987/199005
Related WPI Acc No: 1997-414930; 1997-502655
XRPX Acc No: N90-028426

Data flow machines for data driven computing - has data driven processor mode architecture using 3 FIFO registers per node with data flow memories and parameter memory

Patent Assignee: AT & T TECHNOLOGIES INC (AMTT); US DEPT ENERGY (USAT)
Inventor: DAVIDSON G S; GRAFE V G
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US N7223133	N	19891121	US 88223133	A	19880722	199005 B
WO 9001192	A	19900208	WO 89US3044	A	19890718	199009
JP 3500461	W	19910131				199111
US 5465368	A	19951107	US 88223133	A	19880722	199550
			US 90559523	A	19900724	

Priority Applications (No Type Date): US 88223133 A 19880722; US 90559523 A 19900724
Cited Patents: US 4591979; US 4675806; US 4809159
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US N7223133	N		82		
WO 9001192	A	E			
Designated States (National): JP					
US 5465368	A		28	G06F-013/00	Cont of application US 88223133

Abstract (Basic): US N7223133 N

The data flow computer includes a number of First-In-First-Out (FIFO) registers, a number of related data flow memories, and a processor. The processor makes the necessary calculations and includes a control unit to generate signals to enable the appropriate FIFO register receiving the result. There are three FIFO registers per node: an input FIFO register to receive input information form an outside source and provide it to the data flow memories; an output FIFO register to provide output information from the processor to an outside recipient; and an internal FIFO register to provide information from the processor back to the data flow memories. The data flow memories are comprised of four commonly **addressed** memories.

A parameter memory holds the A and B parameters used in the calculations; an opcode memory holds the instruction; a target memory holds the output **address** ; and a tag memory contains status bits for each parameter. One status bit indicates whether the corresponding parameter is in the parameter memory and one status but to indicate whether the stored information in the corresponding data parameter is to be reused. The tag memory outputs a 'fire' signal (signal R VALID) when all of the necessary information has been stored in the data flow memories, and thus when the instruction is ready to be fired to the processor.

ADVANTAGE - Executes instructions as soon as they arrive at the processor **without waiting** for further **data** or **instruction** fetches.

Dwg.1/11
US 7223133 N

The data flow computer includes a number of First-In-First-Out (FIFO) registers, a number of related data flow memories, and a processor. The processor makes the necessary calculations and includes a control unit to generate signals to enable the appropriate FIFO register receiving the result. There are three FIFO registers per node: an input FIFO register to receive input information form an outside source and provide it to the data flow memories; an output FIFO register to provide output information from the processor to an outside recipient; and an internal FIFO register to provide information from the processor back to the data flow memories. The data flow memories are comprised of four commonly **addressed** memories.

A parameter memory holds the A and B parameters used in the calculations; an opcode memory holds the instruction; a target memory holds the output **address** ; and a tag memory contains status bits for each parameter. One status bit indicates whether the corresponding parameter is in the parameter memory and one status but to indicate whether the stored information in the corresponding data parameter is to be reused. The tag memory outputs a 'fire' signal (signal R VALID) when all of the necessary information has been stored in the data flow memories, and thus when the instruction is ready to be fired to the processor.

ADVANTAGE - Executes instructions as soon as they arrive at the processor **without waiting** for further **data** or **instruction** fetches.

Dwg.1/11
US 7223133 A

The data flow computer includes a number of First-In-First-Out (FIFO) registers, a number of related data flow memories, and a processor. The processor makes the necessary calculations and includes a control unit to generate signals to enable the appropriate FIFO register receiving the result. There are three FIFO registers per node: an input FIFO register to receive input information form an outside source and provide it to the data flow memories; an output FIFO register to provide output information from the processor to an outside recipient; and an internal FIFO register to provide information from the processor back to the data flow memories. The data flow memories are comprised of four commonly **addressed** memories.

A parameter memory holds the A and B parameters used in the calculations; an opcode memory holds the instruction; a target memory holds the output **address** ; and a tag memory contains status bits for each parameter. One status bit indicates whether the corresponding parameter is in the parameter memory and one status but to indicate whether the stored information in the corresponding data parameter is to be reused. The tag memory outputs a 'fire' signal (signal R VALID) when all of the necessary information has been stored in the data flow memories, and thus when the instruction is ready to be fired to the processor.

ADVANTAGE - Executes instructions as soon as they arrive at the processor **without waiting** for further **data** or **instruction** fetches.

Dwg.1/11

Title Terms: DATA; FLOW; MACHINE; DATA; DRIVE; COMPUTATION; DATA; DRIVE; PROCESSOR; MODE; ARCHITECTURE; FIFO; REGISTER; PER; NODE; DATA; FLOW; MEMORY; PARAMETER; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-013/00
International Patent Class (Additional): G06F-009/30; G06F-015/82
File Segment: EPI

14/5/32 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007238427

File Segment: EPI

14/5/33 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004763371
WPI Acc No: 1986-266712/198641
XRPX Acc No: N86-199319

Buffer memory control system for executing immediate instruction - has block fetch control unit to generate move-in complete signal for heading sub-block to start store operation

Patent Assignee: FUJITSU LTD (FUJT)
Inventor: OSONE H; SHINOHARA T
Number of Countries: 010 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 196970	A	19861008	EP 86400641	A	19860326	198641	B
AU 8655009	A	19861002				198652	
BR 8601389	A	19861202				198703	
ES 8800480	A	19880101	ES 553491	A	19860326	198809	
US 4737908	A	19880412	US 86844688	A	19860327	198817	
CA 1250053	A	19890214				198909	
KR 9005420	B	19900730				199140	
EP 196970	B1	19920715	EP 86400641	A	19860326	199229	
DE 3685976	G	19920820	DE 3685976	A	19860326	199235	
			EP 86400641	A	19860326		

Priority Applications (No Type Date): JP 8565620 A 19850329
Cited Patents: 1.Jnl.Ref; A3...8913; EP 54888; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 196970	A	E	25		
Designated States (Regional): DE FR GB SE					
EP 196970	B1	E	17	G06F-012/08	
Designated States (Regional): DE FR GB SE					
DE 3685976	G			G06F-012/08	Based on patent EP 196970

Abstract (Basic): EP 196970 B

The system comprises a central processing unit and a main memory. The central processor has a buffer memory for storing a copy of a portion of the main memory. A buffer control unit is operatively connected to the buffer memory to control a read/write operation. An instruction unit provides an instruction of a type for reading data from and **address** in the main memory and subsequent writing of calculation results. An executing unit executes the calculation.

The buffer memory has a comparator to detect whether or not the data in question is present. If the data is not present a block of data is fetched including the data from the main memory unit by unit. Generation of a move-in complete signal indicates that the move-in of the Leading Subblock from the main memory to the buffer is completed.

ADVANTAGE - Shortens processing time of immediate instruction.

(25pp

Title Terms: BUFFER; MEMORY; CONTROL; SYSTEM; EXECUTE; IMMEDIATE; INSTRUCTION; BLOCK; FETCH; CONTROL; UNIT; GENERATE; MOVE; COMPLETE; SIGNAL; HEADING; SUB; BLOCK; START; STORAGE; OPERATE
Derwent Class: T01
International Patent Class (Main): G06F-012/08
International Patent Class (Additional): G06F-013/16; G11C-011/00
File Segment: EPI

```
Set     Items   Description
S1    7525539   OPERATION? OR FUNCTION? OR INSTRUCTION? OR EXECUTION? OR C-
            OMMAND?
S2     251349   S1 (2N)(FILE? ? OR DATABASE OR DATA()BASE OR INFORMATION OR
             DATA OR LOOKUP OR LOOK()UP)
S3      58738   (WITHOUT OR "NOT")()(SUSPEND? OR DELAY? OR HOLD? OR DEFER?
            OR STAY? OR TABLE? OR WAIT? OR SHELV?)
S4    2200081   S1 (2N)(TASK? OR JOB OR JOBS OR FUNCTION? OR ROLE? OR ASSI-
            GNMENT? OR CHORE? OR DUTY OR DUTIES)
S5    2546205   URL OR URLS OR (UNIVERSAL OR UNIFORM)()RESOURCE()LOCATOR? -
            OR NAMESPACE OR DOMAIN OR ADDRESS? OR FILE()PATH?
S6     346148   S1 (2N) (EXECUTION? OR ATOMIC? OR TRANSACTION? OR ACTIVIT?)
S7          1   S2 (S) S3 (S) S4 (S) S5 (S) S6
S8         41   S2 (S) S3 (S) S4
S9          4   S8 (S) S5
S10         2   S8 (S) S6
S11       110   S2 (S) S3
S12        12   S11 (S) S5
S13         1   S12 (S) S6
S14        13   S7 OR S9 OR S10 OR S12 OR S13
S15        12   S14 NOT PY>2000
S16         7   S15 NOT PD>20000824
S17         7   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/Jun 08
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/May W5
         (c) 2004 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 09
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/May W5
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 08
         (c) 2004 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2004/Jun 09
         (c) 2004 McGraw-Hill Co. Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jun 07
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 08
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Jun 09
         (c) 2004 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2004/Jun 09
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Jun
         (c) 2004 The HW Wilson Co
```

17/5,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01985098 SUPPLIER NUMBER: 18706752 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Patent watch. (News Briefs)
Belgrad, Rich
Microprocessor Report, v10, n12, p18(1)
Sep 16, 1996
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 603 LINE COUNT: 00059

FILE SEGMENT: CD File 275

... A branch-prediction cache stores the target instruction and next sequential instruction and is tagged by the **address** of the branch instruction, as in the prior art. In addition, however, the branch-prediction cache also stores the length of the first and second instructions and the **address** of the second **instruction** . This additional **data** allows the target and next sequential instructions to be directly aligned and presented to the parallel decoding circuits **without waiting** for a calculation of their lengths and starting **addresses** .
5,511,212
Multiclock SIMD computer and instruction-cache enhancement thereof
Issued: April 23, 1996
Inventor: Todd...

17/5,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01297489 SUPPLIER NUMBER: 07294202 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Caching catches a ride on 32-bit designs. (technical)
Furlow, Bill
ESD: The Electronic System Design Magazine, v19, n5, p36(7)
May, 1989
DOCUMENT TYPE: technical ISSN: 0893-2565 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2930 LINE COUNT: 00222

ABSTRACT: Semiconductor manufacturers use caching to gain maximum mainframe-level performance from microprocessor design. Intel's and Motorola's new Controlled Instruction Set Computer (CISC) and Reduced Instruction Set Computer (RISC) chips implement cache management via on-chip cache memory. Both Intel's CISC 486 and Motorola's CISC 68040 include bus-snooping logic to maintain the integrity of data as it is passed between cache and main memory. Intel's RISC i860 also uses cache controller functions with virtually addressed instructions. Caching became necessary in microprocessor systems when clock speeds topped 16MHz. Use of a cache in static random-access memory allows less-costly dynamic random-access memory to be used for the main memory.
CAPTIONS: Intel's 32-bit 486 CISC processor (chart); Motorola's 68040 (chart); Set associativity (chart); In wait states, 386 system performance for the Austek A28285 microcache (chart)

SPECIAL FEATURES: illustration; chart
COMPANY NAMES: Motorola Inc.--Product development; Intel Corp.--Product development
DESCRIPTORS: Complex-Instruction-Set Computers; RISC; Microprocessor; Circuit Design; DRAM; Cache Memory; RAM; 32-Bit; Integrated Circuits
SIC CODES: 3674 Semiconductors and related devices
TICKER SYMBOLS: MOT; INTC
TRADE NAMES: Intel 80486 (Microprocessor)--Design and construction; Motorola 68040 (Microprocessor)--Design and construction; Intel 80860 (Microprocessor)--Design and construction
FILE SEGMENT: CD File 275

... to the 030 implies a two-level cache design. The 030 has 256 bytes each for the **data** and the **instruction** cache. The 030's on-chip MMU is a subset of the 68851 paged memory management unit (PMMU) developed for the 68000 family. The MMU translates virtual **addresses** from the CPU to physical memory **addresses** . A separate MMU imposes delays during this translation, so that an MMU placed between the processor and...
...When the MMU is on the processor chip, as it is with the 030 and the 386, **address** translation times are reduced, and real, or physical, caches are used **without** **wait** -state penalties.
Write Strategies and Snooping
When the processor modifies information in the cache, the changes must...

17/5,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01247038 SUPPLIER NUMBER: 06643902 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Design a virtual cache memory with programmable logic arrays.
Frink, Craig
Electronic Design, v36, n17, p125(5)
July 28, 1988
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2430 LINE COUNT: 00190

CAPTIONS: The cache-memory subsystem in Apollo's DN4000. (chart); The cache design & control functions are partitioned into functional groups. (chart); The virtual cache is organized as 2048 lines, containing 4 bytes. (chart); Diagram of master cache controller's state. (chart)

SPECIAL FEATURES: illustration; chart
COMPANY NAMES: Apollo Systems Div.--Innovations
SIC CODES: 3571 Electronic computers
FILE SEGMENT: TI File 148

... detected, the cache controller initiates a cache invalidate cycle on the prematurely updated cache entry.
If an **address** -tag match doesn't occur at the beginning of a write **operation** , the **data** field in the cache line isn't immediately updated. If the PMMU shows that the write operation...

...is set, causing subsequent write operations to this cache line to be captured in the write buffer **without** **waiting** for PMMU validation.
The master cache controller's state diagram describes all the stimulus required to cause...

17/5,K/6 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03269820 Supplier Number: 46711179 (THIS IS THE FULLTEXT)
Patent Watch
Microprocessor Report, v10, n12, pN/A
Sept 16, 1996
ISSN: 0899-9341
Language: English Record Type: Fulltext
Document Type: Newsletter; Refereed; Trade
Word Count: 624
TEXT:
The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.
5,513,330
Apparatus for superscalar instruction predecoding using cached

instruction lengths

Issued: April 30, 1996

Inventor: David R. Stiles

Assignee: NexGen

Filed: October 27, 1993

Claims: 3

In a superscalar pipelined processor with variable-length instructions, circuitry is provided to determine the length of two instructions in parallel and align them. Parallel decoding circuitry is provided for decoding and executing the two instructions. A branch-prediction cache stores the target instruction and next sequential instruction and is tagged by the **address** of the branch instruction, as in the prior art. In addition, however, the branch-prediction cache also stores the length of the first and second instructions and the **address** of the second **instruction** . This additional **data** allows the target and next sequential instructions to be directly aligned and presented to the parallel decoding circuits **without** **waiting** for a calculation of their lengths and starting **addresses** .

5,511,212

Multiclock SIMD computer and instruction-cache enhancement thereof

Issued: April 23, 1996

Inventor: Todd E. Rockoff

Assignee: None

Filed: August 6, 1993

Claims: 24

A SIMD computer typically comprises one or more single-chip processing element (PE) modules, each having one or more PEs and interfaces to multichip subsystems (MCSs). The PEs are responsible for execution, while MCSs coordinate the PEs. One aspect of the invention augments the PE module with multiple clocks to regulate each PE and each MCS at its maximum rate. This invention gives the PE modules the ability to store and repeat instruction sequences at the highest possible rate within the PEs.

5,511,175

Method and apparatus for store-into-instruction-stream detection and maintaining branch-prediction-cache consistency

Issued: April 23, 1996

Inventors: John G. Favor, et al

Assignee: NexGen

Filed: October 20, 1994

Claims: 11

A branch-prediction cache (BPC) includes a tag identifying the address of branch instructions, a record of the last target of each branch instruction, and a copy of the first several instructions beginning at this target address. A separate instruction cache is provided for normal execution of instructions. The instruction cache monitors the system bus for attempts to write to the address of an instruction contained in the instruction cache. Upon such a detection, that entry in the instruction cache and in the BPC is invalidated.

5,509,130

Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor

Issued: April 16, 1996

Inventors: Richard D. Trauben, et al

Assignee: Sun

Filed: December 14, 1994

Claims: 12

A pipelined processor includes an instruction queue and an instruction-control unit to group and issue instructions in a single clock cycle for execution. Integer and floating-point function units capable of providing multiple results per clock cycle are also provided. The instruction queue stores sequential instructions of a program and target instructions of a branch instruction of the program, fetched from the instruction cache. The instruction-control unit decodes the instructions, detects operands cascading from instruction to instruction, and groups instructions.

5,509,129

Long instruction word controlling plural independent processor operations

Issued: April 16, 1996

Inventors: Karl M. Guttag, et al

Assignee: None

Filed: November 30, 1993

Claims: 117

A data processor that operates on instructions controlling multiple processor actions. Each instruction includes a data-unit section and an independent data-transfer section. The data-unit section includes a data-operation field that indicates the type of arithmetic-logic-unit operation and six operand fields. The six operand fields include four source-data register fields and two destination-register fields. The data unit includes a multiplication unit and an arithmetic logic unit. The data unit may include a barrel rotator for one input of the arithmetic logic unit.

PUBLISHER NAME: MicroDesign Resources, Inc.

INDUSTRY NAMES: BUSN (Any type of business); CMPT (Computers and Office Automation)

... A branch-prediction cache stores the target instruction and next sequential instruction and is tagged by the **address** of the branch instruction, as in the prior art. In addition, however, the branch-prediction cache also stores the length of the first and second instructions and the **address** of the second **instruction** . This additional **data** allows the target and next sequential instructions to be directly aligned and presented to the parallel decoding circuits **without waiting** for a calculation of their lengths and starting **addresses** .

5,511,212

Multiclock SIMD computer and instruction-cache enhancement thereof

Issued: April 23, 1996

Inventor: Todd...